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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GEIB, BENJAMIN P	

ART UNIT	PAPER NUMBER
2181	

DATE MAILED: 09/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/754,550	CHO, JANG-HO	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

FRITZ FLEMING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100
9/15/2006

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-21 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as received on 07/05/2006.

Withdrawn Objections

3. Applicant, via amendment, has overcome the objection to the title set forth in the previous Office Action. Consequently, this objection has been withdrawn by the examiner.

Maintained Rejections

4. Applicant has failed to overcome the 35 U.S.C. 102 rejections set forth in the previous Office Action for claims 1-21. Therefore, these rejections are respectfully maintained by the examiner and copied below for applicant's convenience.

Maintained Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-21 are rejected under 35 U.S.C. 102(b) as being anticipated by Emer et al., U.S. Patent No. 6,073,159 (Herein referred to as Emer)

7. Referring to claim 1, Emer has taught a multi-threaded processor, comprising:

a processing pipeline *[CPU; Fig. 1, component 12]* including a number of stages *[column 3, lines 48-51]*, each stage processing at least one instruction, each instruction belonging to one of a plurality of threads *[column 5, lines 31-46]*; and

a fetch unit *[Fig. 2, component 20]* forming one of the stages of the pipeline *[fetch stage; Fig. 3, component 42]* and determining from which thread to fetch an instruction for processing by the processing pipeline *[column 3, lines 62-67]*, the fetch unit receiving information from at least one other stage of the processing pipeline and determining a processing time of the processing pipeline occupied by each thread based on the received information *[The fetch unit receives thread attribute information and determines an estimated processing time of each thread (column 6, lines 22- 45)]*, the fetch unit determining from which thread to fetch an instruction for processing by the processing pipeline based on the determined processing time for each thread *[Instructions are fetched from the thread determined to have the most beneficial estimated processing time (column 6, lines 22-45)]*.

8. Referring to claim 2, has taught the processor of claim 1, wherein the fetch unit determines the thread having the smallest determined processing time as the thread from which to fetch an instruction for processing *[The thread determined to have the fewest data caches misses and, therefore, the smallest determined processing time is selected as the thread from which to fetch (column 7, line 65 – column 8, line 8)]*.

9. Referring to claim 3, has taught the processor of claim 1, wherein the received information includes the operation type of instructions in the processing pipeline *[The*

operation type is used to determine if an instruction in the pipeline is a branch (column 9, lines 1-15)].

10. Referring to claim 4, has taught the processor of claim 3, wherein the received information further includes the operation type of instructions leaving the processing pipeline *[The operation type is used to determine if an instruction leaving the queue stage of the pipeline is a branch (column 9, lines 1-15)].*

11. Referring to claim 5, has taught the processor of claim 4, wherein the fetch unit includes a counter associated with each thread *[column 8, lines 35-39]*, each counter being incremented by a processing time associated with each instruction of the associated thread in the processing pipeline and being decremented by a processing time associated with each instruction of the associated thread leaving the processing pipeline *[For each instruction of a thread in the pipeline a bit in the thread's bit vector is set, thereby incrementing the tally counter associated with the thread by one (a processing time unit). Similarly, for each instruction of a thread leaving the pipeline a bit in the thread's bit vector is cleared, thereby decrementing the tally counter associated with the thread by one (column 9, line 62 – column 10, line 9)].*

12. Referring to claim 6, has taught the processor of claim 5, wherein the fetch unit determines the thread associated with the counter having a smallest count value as the thread from which to fetch an instruction for processing *[column 10, lines 7-9].*

13. Referring to claim 7, has taught the processor of claim 1, wherein the fetch unit generates a weighted instruction count for each thread as the determined processing time of each thread *[column 13, lines 54-67]*, the weighted instruction count for a thread

is a count of the instructions for the thread in the processing pipeline with each instruction weighted by the cycle counts *[constants C_n]* associated with processing the instruction *[column 13, line 66 – column 14, line 26].*

14. Referring to claim 8, has taught the processor of claim 7, wherein the fetch unit includes a counter associated with each thread *[column 8, lines 35-39]*, each counter being incremented by the cycle counts associated with each instruction of the associated thread in the processing pipeline and being decremented by the cycle counts associated with each instruction of the associated thread leaving the processing pipeline *[For each instruction of a thread in the pipeline a bit in the thread's bit vector is set, thereby incrementing the tally counter associated with the thread by cycle counts (after weighting). Similarly, for each instruction of a thread leaving the pipeline a bit in the thread's bit vector is cleared, thereby decrementing the tally counter associated with the thread by cycle counts (column 9, line 62 – column 10, line 9)].*

15. Referring to claim 9, has taught the processor of claim 8, wherein the fetch unit determines the thread associated with the counter having a smallest count value as the thread from which to fetch an instruction for processing *[column 10, lines 7-9].*

16. Referring to claim 10, has taught the processor of claim 1, wherein the processing pipeline comprises:

an instruction decoder *[Fig. 2, component 26]* decoding instructions, which the fetch unit determines to fetch *[column 4, lines 30-31]*, to generate at least an operation type of the instruction as decoder information *[The op code (i.e. operation type) is generated from the instruction code; column 4, lines 31-35]*; and

a queue *[instruction queue; Fig. 2, component 30]* storing the decoded instructions and issuing decoded instructions to an execution unit for execution *[column 4, lines 54-64]*.

17. Referring to claim 11, has taught the processor of claim 10, wherein the received information is the decoder information and the issued decoded instructions *[column 9, lines 1-15]*.

18. Referring to claim 12, has taught the processor of claim 1, wherein the processing pipeline further comprises:

an instruction cache *[Fig. 2, component 24]* storing instructions, and outputting an instruction to the instruction decoder based on which instruction the fetch unit determines to fetch *[column 3, lines 58-61]*; and

an address renamer *[register renamer; Fig. 2, component 28]* mapping a logical address generated by the instruction decoder for an instruction into a real address of a memory device in an execution unit *[The register renamer maps a logical register number (i.e. logical address) into a physical register number (i.e. real address); column 4, lines 43-53]*.

19. Referring to claim 13, given the similarities between claim 1 and claim 13 the arguments as stated for the rejection of claim 1 also apply to claim 13.

20. Referring to claim 14, given the similarities between claim 2 and claim 14 the arguments as stated for the rejection of claim 2 also apply to claim 14.

21. Referring to claim 15, given the similarities between claim 3 and claim 15 the arguments as stated for the rejection of claim 3 also apply to claim 15.

22. Referring to claim 16, given the similarities between claim 4 and claim 16 the arguments as stated for the rejection of claim 4 also apply to claim 16.

23. Referring to claim 17, given the similarities between claim 5 and claim 17 the arguments as stated for the rejection of claim 5 also apply to claim 17.

24. Referring to claim 18, given the similarities between claim 6 and claim 18 the arguments as stated for the rejection of claim 6 also apply to claim 18.

25. Referring to claim 19, given the similarities between claim 7 and claim 19 the arguments as stated for the rejection of claim 7 also apply to claim 19.

26. Referring to claim 20, given the similarities between claim 8 and claim 20 the arguments as stated for the rejection of claim 8 also apply to claim 20.

27. Referring to claim 21, given the similarities between claim 9 and claim 21 the arguments as stated for the rejection of claim 9 also apply to claim 21.

28. Claims 1 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Borkenhagen et al., U.S. Patent No. 6,076,157 (Herein referred to as Borkenhagen).

29. Referring to claim 1, Borkenhagen has taught a multi-threaded processor, comprising:

a processing pipeline *[processor core; Fig. 1, component 100]* including a number of stages *[The processor core is pipelined (column 7, lines 15-17), which, by definition, inherently necessitates a number of stages]*, each stage processing at least

one instruction, each instruction belonging to one of a plurality of threads *[column 7, lines 61-67]*; and

a fetch unit *[instruction unit; Fig. 2, component 220]* forming one of the stages of the pipeline and determining from which thread to fetch an instruction for processing by the processing pipeline *[column 7, lines 61-67]*, the fetch unit receiving information from at least one other stage of the processing pipeline and determining a processing time of the processing pipeline occupied by each thread based on the received information *[The thread switch time-out register, which is part of the instruction unit (column 9, lines 29-33), determines the allowed amount of processing time of the processing pipeline occupied by each thread (column 14, lines 51-55) based upon a value received (i.e. information received) and loaded into the thread switch time-out register; See column 15, lines 1-22]*, the fetch unit determining from which thread to fetch an instruction for processing by the processing pipeline based on the determined processing time for each thread *[When the determined processing time is zero (i.e. the thread switch time-out register is zero), a thread switch occurs and the instruction unit determines to fetch from another thread; See column 15, lines 1-22].*

30. Referring to claim 13, Borkenhagen has taught a method of fetching instructions for processing in a multi-threaded processor, comprising:

receiving, at a fetch unit of a processing pipeline *[processor core; Fig. 1, component 100]*, information from at least one other stage of the processing pipeline *[A value to loaded into the thread switch time-out register; See column 15, lines 1-22]*, the processing pipeline including a number of stages *[The processor core is pipelined*

(column 7, lines 15-17), which, by definition, inherently necessitates a number of stages], each stage processing at least one instruction, each instruction belonging to one of a plurality of threads *[column 7, lines 61-67]*;

first determining a processing time of the processing pipeline occupied by each thread based on the received information *[The thread switch time-out register, which is part of the instruction unit (column 9, lines 29-33), determines the allowed amount of processing time of the processing pipeline occupied by each thread (column 14, lines 51-55) based upon value loaded into the thread switch time-out register; See column 15, lines 1-22]*; and

second determining from which thread to fetch an instruction for processing by the processing pipeline based on the determined processing time for each thread *[When the determined processing time is zero (i.e. the thread switch time-out register is zero), a thread switch occurs and the instruction unit determines to fetch from another thread; See column 15, lines 1-22].*

Response to Arguments

31. Applicants arguments filed on July 5, 2006, have been fully considered but they are not found persuasive.

32. Applicant argues the novelty/rejection of claims 1-21 on pages 7-8 of the remarks, in substance that:

> "The Examiner's quoted passage fails to teach or suggest that the fetch unit receives any information from any other stage of the processing pipeline. As can be seen in Fig. 2 of Emer et al., none of the stages in the processing pipeline transmits information back to the fetch unit" (bottom of page 7 through top of page 8)

These arguments are not found persuasive for the following reasons:

The fetch unit selects from among multiple program counters (i.e. threads) instructions to fetch (column 3, lines 62-67). This selection is done responsive to thread attribute information collected for each thread (column 6, lines 22-45). This thread attribute information comes from other stages. For example, under the BRCOUNT selection scheme, the number of branch instructions in the decode, rename, and queue stages are counted (column 7, lines 51-64). In order for the number of branches within a particular stage to be counted, branches must be counted during, or within, that particular stage. Since this counting is done in the above-mentioned stages, thread attribute information is received from these stages.

33. Applicant argues the novelty/rejection of claims 1 and 13 on pages 8-9 of the remarks, in substance that:

> "a thread switch time-out register 430 is part of thread switch logic 400, and not part of an instruction unit 220, as alleged by the Examiner" (top of page 9)
>
> "nowhere in Borkenhagen et al. does it disclose that the thread switch time-out value is received by the instruction unit, nor does it disclose that the instruction unit use the information to determine a processing time of the pipeline occupied by each thread" (1st full paragraph on page 9)

These arguments are not found persuasive for the following reasons:

In response to Applicant's argument that the thread switch time-out register is not part of the instruction unit, the Examiner notes that the thread switch logic, which includes the thread switch time-out register, is included in the instruction unit, but that for ease of explanation the thread switch logic has been illustrated external to the instruction unit (See column 9, lines 29-34). Since the thread switch time-out register is

included in the instruction unit, the thread switch time-out value is received by the instruction unit.

The thread switch time-out register, part of the instruction unit, determines the amount of time a specific thread has left to execute before a thread switch is forced (column 14, lines 51-55). This amount of time is the allowed amount of processing time of the processing pipeline occupied by each thread. Therefore, the thread switch time-out register determines a processing time (i.e. the allowed time) of the processing pipeline occupied by each thread.

Conclusion

34. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

35. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or

patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz Fleming can be reached on (571) 272-4145. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

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9/15/2006